Electronic Version

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[ESD DESIGN, VERIFICATION AND CHECKING SYSTEM AND METHOD OF USE]

Abstract

A computerized method and system for designing, verification and checking of the electrostatic discharge (ESD) protection circuits and their implementation in a integrated computer chip design where the computer chip comprises of electronic circuits designed in a parameterized cell design system, pads, interconnects and the ESD system uses a hierarchical system of parameterized cells (p-cells) which are constructed into higher level ESD networks. Lowest order p-cells pass user defined parameters to higher order p-cells to form an ESD protection circuit meeting design criteria. Ones of the p-cells are "grow-able" such that they can form repetition groups of the underlying p- cell element to accommodate the design parameters. Layout and circuit schematics are auto-generated with the user varying the number of elements in the circuit by adjusting the input parameters. The circuit topology automation allows for the customer to auto generate new ESD circuits and ESD power clamps without additional design

work.